**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1 – 10 (Canceled)

11. (original) A power enhanced lateral DMOS device comprising:

a semiconductor substrate, the semiconductor substrate including a plurality of source/body structures thereon; and

a slot on the semiconductor substrate between the plurality of source/body structures to provide a truncated source, the slot oxidized, and

a metal within the slot to provide a ground strap shorting the source to body to ground.

12. (original) The LDMOS device of claim 11 wherein the semiconductor substrate comprises:

a substrate region; and a buried layer, or Boron Up Diffusion where required and

an epitaxial (EPI) layer over the substrate region, wherein the source/body structures are provided in the EPI layer.

13. (original) The LDMOS device of claim 11 wherein the truncated source and the ground strap shortens the path from the source/body junction to ground and reduces voltage drop that occurs as a result of current flow induced by impact ionization in the source/body junction.

14. (original) The LDMOS device of claim 11 wherein snap back voltage is enhanced to a higher breakdown voltage due to reduced NPN action in the ground/body/epitaxial parasitic NPN transistor.

15. (original) The LDMOS device of claim 11 wherein the structure is oxide isolated.

16. (original) The LDMOS device of claim 11 wherein the metal comprises a first and second metal that can be provided with single metal patterning and etching for the interconnect.

17. (original) The LDMOS device of claim 16 wherein the first and second metals can be thick as compared to standard approaches which would result in metal breakage.